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FADC-based DAQ for HiRes Fly's Eye

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Abstract

This paper describes a data acquisition system for optical telescopes studying extensive air showers for the High Resolution Fly's Eye Project at Dugway Proving Grounds, Utah. The measurements are based entirely on flash-analog-to-digital conversion of phototube signals, digitized continuously at 10 MHz, and stored in a deep (820 μs) pipeline, for deadtimeless readout following a parallel pipeline trigger. The massive parallel processing by digital signal processors and programmable logic devices is distributed site-wide, with 42 telescopes and a central facility linked by optical fiber. The system was designed and built at Columbia University, Nevis Laboratories. © 2002 Elsevier Science B.V. All rights reserved.

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1. Introduction

The High Resolution Fly's Eye Project (HiRes) detects and reconstructs the extensive air showers produced when 10^{18}–10^{21} eV cosmic rays interact in the earth's atmosphere, by observing the ultra-violet fluorescence and Cherenkov radiation produced by charged particles in the shower. The detector consists of 64 optical telescopes at two sites in the desert of western Utah. Each telescope is a mirror with collecting area $4\,m^2$. At the focal plane of each mirror is a 16×16 array of hexagonal photomultiplier tubes, each forming a pixel of about 1°. Twenty-two mirrors are located at the site of the original Fly's Eye experiment: Five Mile Hill at Dugway Proving Grounds, Utah, with instrumentation previously designed at the University of Utah. This paper describes the data acquisition system for the 42 telescopes located 13 km away on Camelsback Ridge and instrumented with a flash analog-to-digital conversion (FADC) system designed and built at Columbia University, Nevis Laboratories.

HiRes extends the techniques developed by the original Fly's Eye Experiment [1] to cosmic ray showers of much greater energy, where lower flux requires measurement at much greater distances, as far as 60 km from the detector. We accomplish this by increasing the collection area of the mirrors to $4\,m^2$, reducing the pixel size to 1°, and continuously digitizing the signals at 10 MHz. The pixel size of 1° provides better spatial

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resolution and limits the noise superimposed on any signal by background light. A typical shower is seen in 10–100 tubes, with signals in each tube ranging from a few to several thousands of photoelectrons in pulses of 0.1–4 μs duration. These showers are detected and measured over a fluctuating background of about 40 photoelectrons per μs per tube, the typical night sky noise on a clear moonless night.

Accurate shower reconstruction requires that the pulse area and time evolution of each signal be measured as well as possible within the constraints of photoelectron statistics. Thus, the electronic noise must be small compared to the night sky background, and the timing resolution should preserve the geometrical information about the longitudinal evolution and shower trajectory. The trigger should be sensitive to any reconstructable shower—typically at least 100 photoelectrons per tube at the peak, and should force readout of all measurable signals associated with that shower. The event rate is small, less than one per minute per mirror for cosmic ray showers. But a realistic trigger sensitive to distant showers is also sensitive to the Cherenkov light from lower energy cosmic rays, closer to one per second per mirror, and to random fluctuations in the night sky background. The FADC trigger may exceed 200 Hz per mirror, mostly random noise triggers. Most uninteresting events are filtered out online, and event readout normally occurs less than once per second per mirror.

The HiRes FADC system continuously digitizes all analog signals at 10 MHz, passing the digitizations through a delay buffer 820 μs deep. The advantages of such immediate analog conversion to deeply buffered digitizations include:

(1) ample delay to form triggers based on distributed digital information;
(2) minimal analog processing, isolated from subsequent digital processing;
(3) trigger based solely on digital processing of FADC measurements;
(4) deadtimeless readout of all channels, from before event to after event.

The instrumentation is required to perform reliably in a remote site with minimal human intervention. The temperature within the mirror buildings ranges from 140°F in summer days to −30°F in winter nights. Severe weather, lightning and AC power problems are commonplace. The AC power to the mirror buildings is in buried cable, from a single three-phase 208VAC uninterruptable power supply with sufficient battery backup power to close the roll-up doors in all mirror buildings. All communications between buildings rely on optical fiber. All wiring and electronics are shielded from rodents.

2. Overview

The 42 telescopes on Camelsback are housed in pairs in 21 mirror buildings, as shown in Fig. 1. The site is laid out like a wheel with a central facility at the hub, distributing a 10 MHz measurement clock and limited central control to mirror buildings along equal length optical fibers. Two more independent optical fiber rings, one in each direction around the circumference and linked to the central facility, provide trigger and data communications between buildings. If the rings are broken by a failure, software-controlled hardware loopback allows efficient operation of all accessible nodes.

The central host computer is a VME PC (Xycom Automation XVME-659), with standard PC hardware: 100 Mbit/s Ethernet, 40 MB/s SCSI interface, serial ports, color graphics and 128 MB

Fig. 1. A view of one of the buildings with the door open.

of memory. The operating system is a standard multi-tasking Linux system that readily allows the allocation of 32 MB of memory for access by a VME master designed at Nevis. This VME interface, the VLink, has flexible high speed access to the memory of the Xycom board, more than 20 MB/s in block transfers initiated by the VLink, requiring no interrupt service by the PC.

The topology of communications is outlined in Fig. 2. The VLink is connected to the optical fiber rings that link the mirror buildings and to two Clock modules over a short cable bus. These Clock modules in the central facility drive optical fibers delivering the 10 MHz clock to each mirror building with equal time delay, and provide synchronous central control (system reset, clock on/off/reset) and program code. Each of the 21 mirror buildings at the Camel's Back site has two telescopes serviced by a single electronics rack containing a small, low-power control crate and two FADC crates. The control crate contains two modules: an MLink module that provides communication links and a Power module that controls power supplies, a heat exchanger in the rack, heaters and programmable test pulsers for

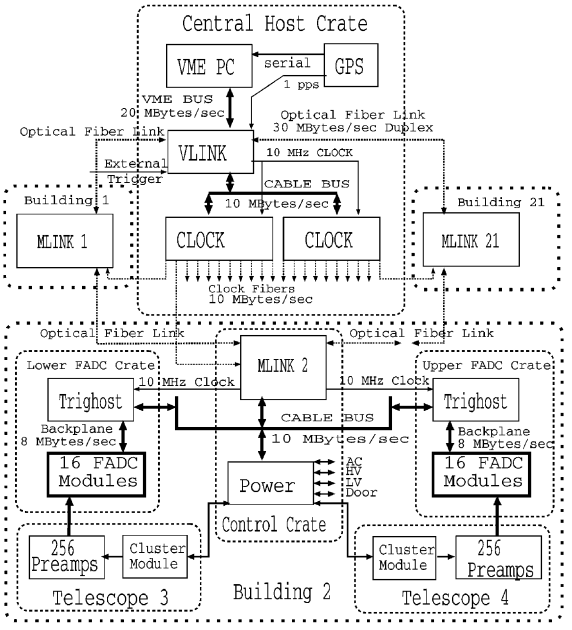

Fig. 2. Communications diagram.

the phototube arrays. It also operates the roll-up doors and monitors temperatures, voltages, light levels and door status. In full operation, the rack uses 1300 W of single phase 208VAC.

Each telescope is a mirror, imaging the night sky onto an array of 256 phototubes: 16 vertical columns by 16 horizontal rows. The tubes are enclosed in a cluster box, with a glass filter that transmits in the near ultraviolet (300–400 nm). The tubes are operated at low gain, typically 10^5, with additional amplification and shaping in the base. The photocathodes are at ground potential, requiring the anode signals to be AC coupled with a 500 μs time constant. A preamp in the base provides differential output voltage equal to twice the anode signal current times 3 kΩ, and has a filter with two 35 ns poles to limit bandwidth and nonlinearity for narrow pulses. The dynamic range of signals on the output cable is defined by electronic noise of less than 0.5 mV and saturation around 4 V.

The cluster box also contains a circuit with a 32-channel programmable test pulser and a variety of monitoring functions, including voltage, temperature and light level. The temperature of the cluster can be stabilized with a software controllable heating strip. The cluster is enclosed to exclude rodents and dust, with temperature uniformity maintained by passive conductivity and convection. Total power dissipation during normal running is 40 W of low voltage power and 60 W of HV, with an additional 100 W available when the heater is enabled.

Phototube signals are transported on equal-length shielded twisted-pair cables to a nearby FADC crate. This crate contains 16 FADC cards, and a Trighost module that provides trigger processing, control and communications. The FADC cards each receive signals from a vertical column of 16 phototubes, digitizing shaped signals from each tube every 100 ns and storing 8-bit numbers in a ring buffer, M1, that provides 820 μs of delay for trigger formation. Each FADC card also processes two analog sums of 16 phototube signals: a vertical column and a horizontal row that provide horizontal and vertical projections of a moving shower image. Each sum is digitized twice, with lower gain to extend the dynamic

range, and with a longer filter time to provide a comparison with an adjustable threshold.

Threshold comparisons are pipelined to the Trighost module for pattern recognition and trigger generation. Triggers are stored in a local trigger queue and also transmitted to neighboring mirrors. Within a single mirror, data transfer from M1 to a second memory, M2, is controlled by the DSP of the Trighost module. The 820 μs delay allows the DSP to combine the triggers from local or distant sources into discrete time intervals to be stored for further processing by fast DSPs on each FADC card, before a final readout decision is formed.

Data stored in response to a pipeline trigger is first scanned for pulses by the DSPs on the FADC cards. If the trigger is confirmed by the detection of a modest number of neighboring pulses, all storage windows associated with the trigger are rescanned, and raw data is read out in the vicinity of detected pulses.

3. Design considerations and performance

3.1. Dynamic range

The dynamic range of the analog-to-digital (ADC) system is less than one might expect to require for measurements of showers spanning more than two decades in energy and with observed intensity varying strongly with distance and shower orientation. Individual channels have 8-bit ADCs and typically have noise fluctuations of 1 to 2 counts (RMS). The range is extended by digitizing row and column analog sums with 8 times lower gain, but even this results in an effective overall dynamic range of only 10 or 11 bits.

Despite the commercial availability of 10- and 12-bit ADCs, we chose 8-bit ADCs after careful simulation of the measurements. The reduced range not only reduces cost and complexity, but also improves the reliability and accuracy of measurements within the lowest 256 bins, where nearly all useful measurements fall.

Detected light intensity decreases rapidly with increasing distance from source to detector, with the inverse square reduction in geometrical acceptance further reduced by exponential attenuation lengths on the order of 10–20 km at lower elevations. Since the volume of observed atmosphere increases rapidly with distance, the majority of the events detected at any energy are at distances comparable to the maximum distance at which signals can be resolved. For each energy increase by a factor of 10, the cosmic ray flux is falling by a factor of 300–1000. Despite a rapid increase in detection efficiency, or aperture, with increasing energy, as we can see brighter showers at greater distances, the spectrum of observed events still falls rapidly with increasing energy. Only a tiny fraction of the reconstructable showers at any energy require the extended range of the low-gain current sums.

The 8-bit AD775 ADC measures a 2-V range in 8 mV steps. In actual operation, the measurements have properly defined binning, stable baseline and negligible electronic noise. Had we chosen a 12-bit ADC with 0.5 mV bins, we could not do as well for the vast majority of all events at all energies that have no signals with more than 200 photoelectrons in a single 100 ns sample.

The dynamic range of the signal at the preamp output cable is roughly 13-bit, with fractional millivolt noise and roughly 4 V saturation. We use some of this range to permit variable gain amplifiers to reduce the gain for high gain tubes at the ADC rather than adjusting the tube gain, shifting the 4 V signal saturation on the preamp cable to lower light levels.

3.2. Photon fluctuations—stars and trigger thresholds

During normal running, on dark clear nights with doors open, tubes typically see 20–40 photoelectrons per μs. The fluctuations in the number of photoelectrons integrated within the filter time cause much larger baseline fluctuations than electronic noise, with a variance roughly equal to the number of photoelectrons in 100 ns.

With a variance of 2–4, we appear to lose at least the lowest order ADC bit, but we also reduce digitization error. Shifting the baseline by a fraction of a bin shifts the observed average by

the same amount in the presence of this noise. The measured area of a slow pulse does not depend on the position of the baseline with respect to bin boundaries—a very important feature for signals that are a few bins above baseline for many samples.

For the row and column sums of 16 tubes, the conversion gain is 8 photoelectrons per ADC bin and the RMS noise has increased four-fold, usually to slightly more than one bin. For the trigger channels, the integration time has increased nearly tenfold, and so we expect RMS fluctuations corresponding to nearly 25 photoelectrons. For normal mid-range trigger channel gains of 2.5 integrated ADC counts per photoelectron, we typically observe trigger channel variances of less than 20.

The fluctuations in the trigger channels determine the practical thresholds for triggering. We fix the thresholds at 12 counts above pedestal, but we prevent the variance from exceeding 20 as light levels increase by reducing the trigger channel gain. The resulting thresholds are approximately 50 photoelectrons for a short pulse in low background light, increasing to 100 photoelectrons for a trigger channel with a very bright source with 48 times the average background light of a single channel, for example a bright planet at high elevation.

This observable noise introduced by statistical fluctuations in arriving photons provides useful information through its indirect measurement of light levels. Stars provide a large number of stable point sources that typically sweep across individual tubes in about 5 min. The light and observed variance may exceed 100 photoelectrons per 100 ns and provide an accurate mapping of the telescope response to a point source, establishing directions with great accuracy and checking the attenuation of light in the atmosphere. Fig. 3 shows the response to a star in the variance of a single tube in a corner of a cluster, where spherical aberration is maximum.

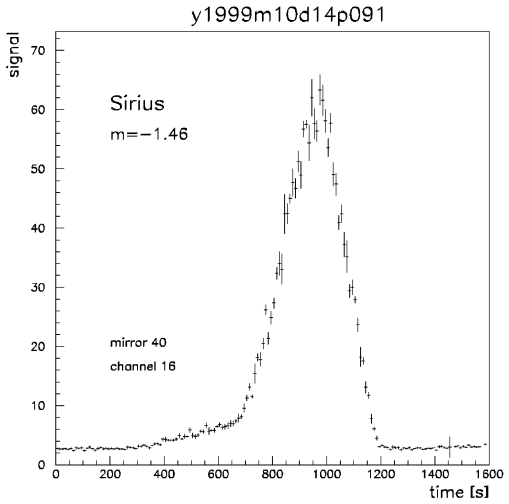

Fig. 3. The star Sirius passing through the field of view of a single tube.

3.3. Electronic noise

In the dark, with doors closed but otherwise in normal running mode, with HV on and overall gains set to one photoelectron per ADC count, the baseline has short term fluctuations of roughly 0.1 ADC bin (RMS). This yields a long series of identical digitizations unless the baseline is near the edge of a bin. We can measure this noise (and the locations of bin boundaries) by sweeping the baseline across the bins in very fine steps, using the 12-bit digital-to-analog converter (DAC). The bin boundaries may differ for alternating measurements in any one channel, since each ADC chip alternates between internal components in a parallel pipeline.

The baseline noise has two comparable sources: the CLC522 variable gain amplifier and noise in the HV. The CLC522 has a relatively high noise factor that we could not improve. It also has modest power supply rejection (meaning its DC output level shifts with the DC power, feeding power supply noise into the signal path), but we reduce power supply noise adequately by providing voltage regulators and filtering in the analog section of the FADC module. Since we operate the tubes with photocathodes at ground, the photomultiplier signals appear as small fluctuations in the anode HV, and therefore HV ripple is indistinguishable from signal. One ADC count represents 8 mV at the ADC, but 0.1 mV at the anode, where the DC voltage is approximately

1 kV. We therefore required sufficient filtering to keep the HV ripple below one part in 10^8 for the time scale between 100 ns and a few hundred μs. The trigger channels see the sum of 16 channels with high gain for slow signals and are therefore quite sensitive to common mode noise introduced by power supplies. Any common mode problem shows up as correlations in trigger channel noise.

Another type of electronic noise is the slow drift of the baseline, which is dominated by the temperature-dependence of the input offset of the final amplifier. Since the AC coupling and baseline offset must be set before this amplifier to allow it to define the output limits, the input offset is multiplied by the gain of 16. For the trigger channels, a baseline drift affects the trigger threshold, but we monitor the pedestals continuously and restore them as they drift. The local DSP provides a simple baseline servo: computing an average of 256 consecutive samples five times per second and changing the pedestal DACs by a maximum of $\frac{1}{16}$ of an ADC bin per sample to compensate for error.

3.4. Signal processing

The photomultiplier tube is a Photonis XP3802: with a flat, hexagonal bialkali photocathode. A single photoelectron signal is about 2 ns wide and has a spread in its total charge that is about 30% (RMS) at a typical gain of just under 10^5. The spread in transit times for the photoelectrons traveling from the flat photocathode to the first dynode is ignored in subsequent filter discussions.

The 256 phototubes within a cluster are operated at one common HV, typically 1 kV. The tube gains are measured before installation into base assemblies. A series resistor in the HV chain that helps form an RC filter for the HV is chosen to make the tube gain approximately the desired value at 1 kV external voltage.

Signals are transported from phototube preamps to ADCs within a nearby rack, using 10 m long shielded twisted pair cables. A variable-gain amplifier in the cable receiver trims the overall response. Analog sums of the 16 individually balanced signals in vertical columns and horizontal rows are digitized with reduced gain and also with higher gain at lower frequencies to provide threshold comparators for trigger generation.

3.4.1. Filter response and baseline restoration

We wish to measure the light intensity, or photoelectron current, to within the accuracy of the photon statistics and the limitations of 100 ns sampling interval. To make the measurement of a charge impulse from the tube be independent of its time with respect to the 10 MHz sampling clock, the impulse response must be smeared out over a wider interval than 100 ns, but not much wider or we lose the time structure.

We have chosen a filter that is dominated by four roughly equal 35 ns poles, two in the preamp and two in the ADC module. The total charge is the sum of the ADC measurements (more than 90% in two or three samples), and varies from the mean by about 5%, as the impulse time varies with respect to the sample time. The mean time of the impulse may be calculated by weighting the sample time with its ADC value, and will correctly track the impulse time within 3 ns, if we can ignore digitizing error. We measure the impulse response of the detector with a laser pulse distributed by quartz fibers to each telescope. The preamp design, including the two filter poles, permits linear response to fast impulses out to saturation of the cable driver. Filtering at the ADC suppresses subsequent high frequency noise, introduced perhaps in cable transmission between separate subsystems.

The phototube signals are superimposed on the 1 kV voltage of the anode, and are therefore AC-coupled to the preamp, with 500 μs time constant. To provide a controllable baseline at the ADC, we AC-couple immediately before the ADC with the same time constant and an average baseline value derived from a 12-bit DAC. The resulting baseline restoration resembles single AC-coupling with 250 μs time constant. At the end of a 5 μs square pulse, the baseline would drop by 2% of the pulse amplitude and pass through the original baseline 1 ms later.

The low-gain analog sums have the same filtering, including baseline restoration, as the individual high-gain channels. The trigger sums have two additions to the overall filter response: an

impulse is stretched to approximately 1 μs by the addition of two more 500 ns filter poles; and the baseline restoration receives an additional 110 μs AC-coupling, which dominates the baseline restoration.

3.4.2. Pipelined pattern recognition—first step in triggering

The image of a distant cosmic ray shower sweeps across a cluster of phototubes along a straight line whose orientation and speed depend on the position and orientation of the shower trajectory. The shower signature is phototube signals that progress in a straight line, progressively disappearing from tubes and appearing in neighboring tubes. We therefore look initially for a pattern of tubes adjacent in space and time, for a wide range of pulse widths and shower directions.

With massive parallel processing, we could search continuously for such patterns in the continuous digitizations of the two-dimensional array of individual tubes, but the task is much easier if we first consider the one-dimensional horizontal and vertical projections provided by the row and column sums. Two disadvantages of this technique are that we combine the noise from 16 tubes, raising the effective threshold by four, and we are restricted to a predefined filter time. On the other hand, summing provides some compensation for the sharing of light between tubes, and a shower with reconstructable trajectory and energy profile has several tubes with varying pulse amplitudes such that a modest number are easily detected.

Simple pipelined logic in programmable logic devices (PLDs) detects adjacent pulses by first doubling the widths of the row and column threshold excursions by using 6-bit counters to extend the pulses by up to 6.4 μs, requiring a coincidence between the doubled pulses and the OR of the undoubled pulses, and then repeating the process to generate a three-fold coincidence. A trigger is two or more different three-fold coincidences, followed by 5 μs without coincidence or 102.4 μs elapsed trigger time. The trigger generates an interrupt to a DSP, which then reads out the times of the first and last coincidences, and the coincidence pattern. This trigger information is stored in a local trigger queue and also transmitted to neighboring mirrors.

3.4.3. Storing a time window

The trigger DSP also specifies the start/stop times for transferring digitizations from the output of the 820 μs delay memory to a second memory for further study and perhaps readout. This storing of a selected window is a software-driven first stage trigger, with a decision based on trigger logic generated in a local or distant telescope, or requests from the central host. All 320 channels within a telescope are stored for the same time interval.

Storage windows cover a time interval centered on the hardware trigger, for a total time span of 3 times the trigger span plus 12.6 μs, with a maximum span of 200 μs. The event buffer can store 3.2 ms, but if any event buffer lacks space for a maximal event, triggers are disabled until all event buffers are empty. Each event buffer has room for more than 100 typical events, but is usually empty or nearly empty.

Starting and stopping a storage interval is synchronized to the 10 MHz measurement clock by the trigger DSP loading the transition time into a PLD register in advance of the specified time. Triggers from multiple sources may be simply combined into one storage window if their implied storage windows overlap or if the start of one window is less than 25.6 μs after the end of the previous, subject to the limitation of 200 μs maximum.

3.4.4. Confirming scan

After a local trigger has been stored, local DSPs scan the event buffer with a single pole digital filter, whose time scale approximates the trigger hardware, and with a threshold less than half the hardware trigger threshold. We scan only the individual tube channels, within a time window bracketing the trigger time. The scan is intended to quickly verify the hardware trigger, and requires the lower threshold to detect a signal split between two tubes. A list of all detected pulses is reported to the trigger DSP, identifying the tube, and the

time and value of its peak response to the filter algorithm.

If at least three signals are found, additional pattern recognition is imposed. An event with a modest number of signals has isolated clusters identified, and usually requires at least one cluster of three neighboring tubes, where neighboring is defined as the six immediate neighbors plus the six next-nearest neighbors that line up with the cracks between nearest neighbors.

At this point, one can effectively discriminate between random noise, track-like showers, relatively symmetric fast blasts of light from low energy showers seen head-on, and a variety of artificial sources ranging from calibration lasers to aircraft.

Confirmation or rejection of a locally generated trigger is broadcast to all recipients of the initial trigger.

3.4.5. Measurement scan and readout

All storage windows associated with confirmed triggers and a prescaled subset of unconfirmed triggers are then fully scanned, with a scanning algorithm that depends on the event classification. Event classifications include: (1) pedestal snapshots, for which we simply calculate the mean and variance of measurements within 25 μs windows 4.8 times per second, reporting up the average of 48 windows every 10 s; (2) tagged calibration events whose signature includes the timing within the gps second; and (3) normal events. For the normal events, we read out the results of the measurement scan and a 10 μs sequence of raw data centered on any signal uncovered in the scan.

3.5. Setting and maintaining a stable calibration

At the beginning of each evening run, the DSPs on the FADC cards first verify digital functions by writing and reading patterns in registers and memory, then with input amplifiers disabled, step the pedestal DACs through their full range to verify the performance of DAC, final amplifier and ADC. A test pattern is next loaded into M1, to test the trigger processing from trigger channel through recording in the central facility.

With pedestals set to normal values, and input amplifiers set to midrange, the pulser in the cluster generates patterns to check the response of individual channels and the linear sums. Since gains are defined by precision resistors and DACs, gains are stable with time and vary by at most a few percent from channel to channel. Gain errors in the pulser test indicate hardware problems requiring attention: usually a faulty component on an easily replaced subassembly.

Next, HV is turned on, and the tubes are illuminated by fast light pulses from a YAG laser [2] whose light is distributed to telescopes by quartz fibers. By separately illuminating different families of fibers, we monitor tube gains and mirror reflectivity. Gain variation in isolated channels at this stage indicates failing phototubes.

Throughout the nightly running, cross checks on gain calibration, geometry and atmospheric conditions are provided by radio-controlled xenon flashers located between the two sites [3], and computer-controlled steerable lasers at each site.

At intervals of several weeks, a stable portable light source [4], mounted reproducibly in a fixture on the mirror axis of each telescope, provides a common absolute calibration for all tubes. The DACs controlling the gains of the input amplifiers are adjusted to yield a uniform response, equal to the average number of photoelectrons expected. The actual number of photoelectrons is determined from photostatistics [5], and the average over all tubes provides a check on the light intensity.

3.6. Air shower examples

We illustrate detection and measurement features with two events. The first shower, shown in Fig. 4, has modest energy and great distance, approaching the limits of measurement. The shower triggered two mirrors, each with 4–6 adjacent trigger channels in coincidence, providing measurable signals in 32 phototubes with a detectable image spanning 22° in 66 μs.

Fig. 4a shows the trigger channel waveforms for five adjacent horizontal trigger channels on a section of the shower. In ADC counts, each waveform has pedestal of 20, threshold of 32 and

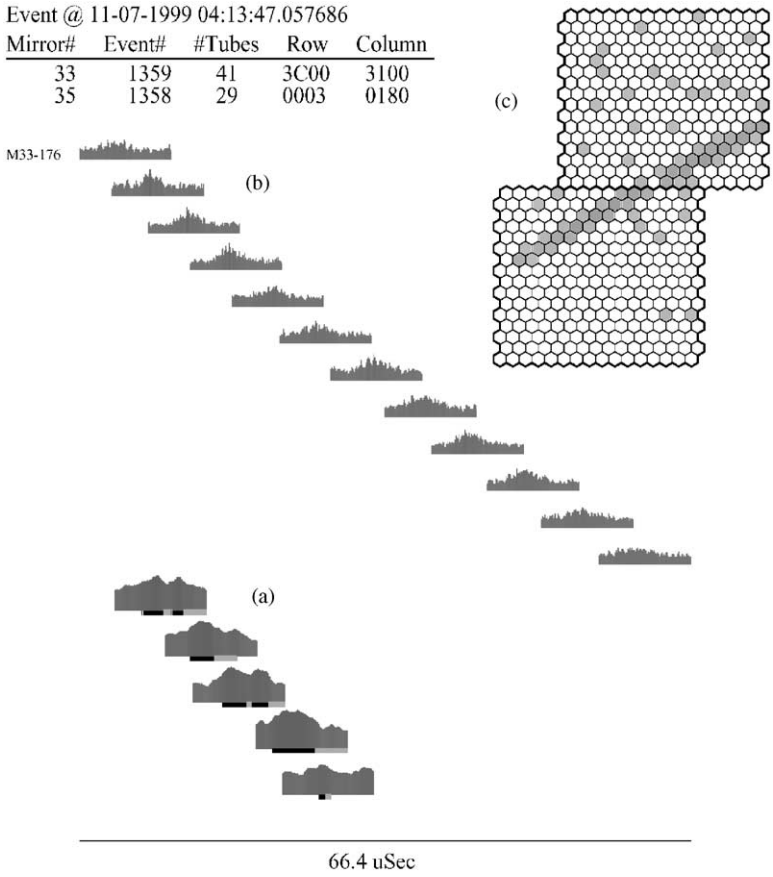

Fig. 4. A distant low energy event passing through two mirrors.

RMS noise of 4 (filtered to μs time scale). Dark bands under the waveforms indicate time above threshold, and the lighter bands indicate the logic extension for coincidences. Both mirrors would have triggered reliably if the shower energy had been only $\frac{2}{3}$ as energetic, but neither would trigger if the event were half as energetic.

In Fig. 4b, we show the waveforms of 12 representative tubes evenly spaced at the center of the shower. A measurement scan of the full storage window forces readout of 10 μs intervals centered on the maximum response above threshold. Each of the waveforms is above the pedestal for at least 4 μs, with a total integrated signal of 200–400 photoelectrons per tube. The RMS fluctuations in the integration range from less than 13 photoelectrons in the absence of any signal but fluctuations in ambient light, to nearly 25 photoelectrons with an expected signal of 400 photoelectrons added to the background.

The positions of recorded tubes within the mirrors is shown in Fig. 4c. The sprinkling of tubes recorded in response to noise fluctuations have small integrated areas and widely varying times.

A second event, shown in Fig. 5, has unusually large signals, with shower energy well above 10^{20} eV and a distance of 27 km from the detector. The initial part of the trajectory is partially obscured by intermediate thin cloud in a rapidly changing atmosphere, but the event is well measured in stereo with adequate monitoring of clouds and atmosphere. Shower maximum is observed by both sites with quite clear air. The

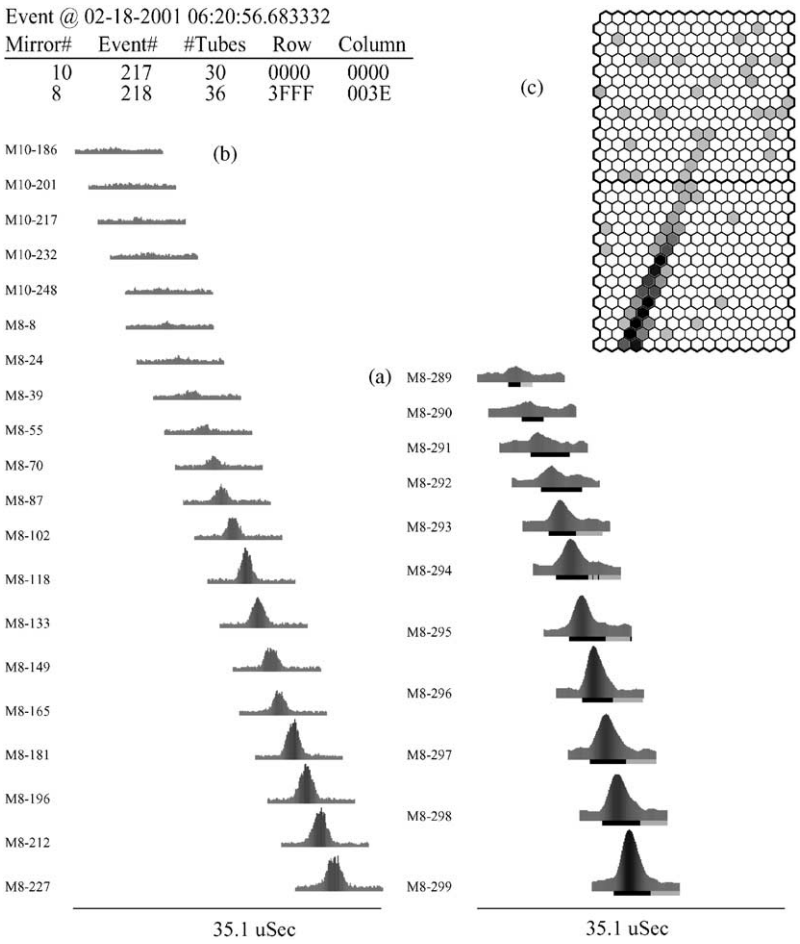

Fig. 5. A nearby high energy event passing through two mirrors.

lower mirror was well triggered and well measured, but the upper mirror failed to trigger on the low light levels transmitted through the cloud.

4. Details of hardware design and operation

Altogether, there are eight different "modules" designed at Nevis to instrument Camelsback:

(1) The FADC module that processes signals from a vertical column of 16 phototubes.
(2) The Trighost module, serving as trigger processor and crate host for an FADC crate.
(3) The MLink module, receiving the 10 MHz clock and characters from the Clock module, linking the buildings with a pair of 30 MB/s serial busses, and providing 256 K words of 16-bit memory for buffering local data.
(4) The Power module, providing control and monitoring functions within a mirror building.
(5) The VLink module, which links a VME host computer to the FADC system.
(6) The Clock module, distributing the 10 MHz clock, central control and Link DSP boot code.
(7) The Cluster module, mounted inside each phototube clusterbox, with a programmable 32-channel test pulser, and monitoring local temperatures, voltages and light levels.

(8) The modular power supply units, providing locally controlled and monitored low-voltage power, compactly, efficiently, inexpensively and without fans.

Most HiRes modules designed at Nevis contain a Motorola DSP56166: a complete 16-bit fixed-point computer, with 2048 16-bit words of program memory and 4096 16-bit words of data memory. In each 33-ns instruction cycle the DSP performs multiple operations, including three memory accesses, one of which may be external. A single cycle multiply-accumulate operation can multiply two 16-bit numbers and add the 32-bit product to a 40-bit accumulator. The DSP has a variety of I/O ports including individually accessible pins, and dedicated external interrupt pins. The chip fits inside a 1 in^2 and consumes much less than a watt. A useful feature for system development is the online debugger port, four pins that can be connected to a PC-based controller. This allows a simple interactive debugger with breakpoints, program load or modification to operate and examine a DSP on a module that may be by itself or installed in a larger system.

The VLink and Trighost modules use the Motorola DSP56309, which is similar in architecture and power consumption, but faster (10 or 12.5 ns instruction cycle) and larger (20K words of 24-bit instruction memory, 14K words of 24-bit data). An internal 6-channel DMA controller is especially useful for the Trighost module, which must communicate simultaneously with the crate backplane and the rack cable bus.

4.1. FADC module

The FADC module is a 4-layer circuit board, 12 in. deep by 12.75 in. high, with ground and power in the interior planes and all signal connections on the outside surfaces. Analog signal processing is restricted to small 2-layer subassemblies at the front of the board, 0.6 in. by 3.3 in., beneath a shield of copper clad circuit board 0.75 in. above the plane of the main board. The analog subassemblies require three different voltages: +4.8 and −4.8 V for the amplifiers and +5.0 V for the DACs and FADCs. Analog ground is connected to the front panel, and thereby to the crate, but the digital ground plane is connected to analog ground only at the crate backplane. The analog power voltages are developed in the analog section, using low-dropout regulators and external power supplies separate from the main digital power.

Each FADC module has a Motorola DSP56166 on a small subassembly near the backplane connector. Before starting normal operations, the DSP verifies all memory locations and data connections, loads a pattern in the first memory to simulate an event which then simulates an incoming pattern and tests the hardware and software from trigger generation to readout. The pedestals, or baselines, of the individual channels can be swept through most of the ADC range to verify much of the analog processing. The DSP provides many initialization functions, serves as a digital signal processor during data taking, and communicates with the Trighost module over the backplane.

4.1.1. Analog section

Differential analog inputs from the phototube cluster are brought into the FADC board on 8-channel DB25 connectors at the top and bottom of the front panel, separated by a 50-conductor flat cable bus for horizontal analog sums. These analog signals are processed with variable gain and offset, controlled by dual 12-bit DACs (AD8522) for each channel. The DACs are loaded with 20 16-bit numbers, using a local DSP serial port. Each 16-bit number is a 12-bit DAC value and 4 control bits. One of the DSP general-purpose I/O pins is pulled momentarily low to load DAC registers after all 20 shift registers are loaded. Offsets and gains are thus loaded separately, requiring approximately 25 μs for each set of 20 numbers. The contents of the DAC shift registers may be read back by the DSP for verification.

The differential analog signal from a phototube is terminated on a subassembly and buffered by a variable gain amplifier (CLC522) whose voltage gain is linear in a controlling voltage between −1 and +1 V, derived from a DAC output (0–4.095 V) and the regulated −4.8 V. The gain-

corrected signal then feeds the horizontal and vertical current sums and is capacitively coupled to a special amplifier (CLC501) for a fixed gain of 16 for digitization by the AD775 A/D converter. The DC offset into this amplifier is controlled by the second DAC output, with a second 500 μs recovery time in addition to the 500 μs time constant introduced by the HV isolation in the tube base. Since the input signal can far exceed the limits for amplification and digitization, the amplifier has been selected for its ability to clamp the output at fixed limits and to recover quickly when the input is again within range.

4.1.2. Digital section

Normal Operation (RUN Mode, 10 MHz clock): The FADC outputs are always enabled and update every cycle of the 10 MHz clock. The FADC output is then loaded each clock cycle into a register R1, which has a fast output enable. A 13-bit counter provides the address for the 8K delay memory M1. For the first 40 ns of each cycle, numbers previously recorded in this location in M1 transfer to a second register R2, for all 20 channels. During the second 40 ns of each cycle, the output of R1 is enabled and written into the current location of M1. The 13-bit address counter is then incremented, providing a new M1 address by the next cycle. This M1 counter is synchronized for all FADC modules with the clock off, so that when the clock is turned on, all M1 counters are the system time, modulo 819.2 μs.

Transfer from R2 to the 32K second memory, M2, is controlled by a STORE level generated by the Trighost module, shipped over the backplane and loaded into a shift register on the FADC card, allowing advance notice to the local DSP that access to M2 is being interrupted. Storage in M2 begins a few cycles later. The DSP receives an interrupt, IRQA, when STORE appears on the board and a second interrupt, IRQB, when STORE disappears. When STORE is present, the address for writing into M2 is a 15-bit counter that increments automatically after each write and is not normally altered by the DSP.

The DSP reads data from M2 only when STORE is absent, by first loading external registers with the channel and starting address. The M2 data can then be read with no wait states, at 10 MHz.

Most of the digital logic on the board is in a single programmable Altera device with 336 logic cells and 160 pins: an EPF8452AQC160. This chip receives the 10 MHz clock, along with five outputs from a tapped delay line (Dallas DS1000-100) providing the clock delayed in 20 ns steps. It also receives STORE and communicates with the local DSP. It generates all distributed clocks, enables, and memory addresses on the board. The actual address lines to M1 and M2 are Gray codes, with only one bit changing when the address increments, to reduce noise and power consumption. All DSP access to the digital section of the board is through this chip, using eight logical addresses and up to 15 bits of the data bus, as described in Table 1.

The control and status register has 13 bits that can be read back from ($A=3$), including channel number, status of STORE, and test mode control bits. To read from these addresses, only the lowest two DSP address bits are used. The third bit, A2, is registered separately by writing 0 or 1 to ($A=1$). For test mode write access to M1, this internal A2 must also be set before writing to ($A=4$), but otherwise the DSP address bit is used for write access. There are three write accesses that do not directly correspond to a read access: ($A=1$) to write internal A2, ($A=3$) to write channel number and ($A=7$) to set test mode control.

In RUN mode, the M1 address counter AQ is incremented by the 10 MHz clock and not synchronized with the DSP. When STORE changes, the value of AQ is recorded so that after

Table 1
DSP access to digital section of FADC module

Address	D[14:0]	
0	0, M2[7:0]	8-bit M2 data, right adjusted
1	0, M2[7:0], 0	8-bit M2 data, shifted left 4
2	RP[14:0]	15-bit M2 DSP read pointer
3	S[12:0]	13-bit status register
4	0, M1[7:0]	8-bit M1 data, right adjusted
5	0, AQ[12:0]	13-bit M1 address counter
6	WP[14:0]	15-bit M2 write pointer
7	(HT,VT,AQ2,AQ1)	Read four 13-bit numbers

STORE disappears the DSP can read four 13-bit numbers from ($A=6$): (HT,VT,AQ2,AQ1) where HT, VT are the running total number of cycles of H, V trigger above threshold at the end of STORE, and AQ1, AQ2 are the values of the M1 counter at the beginning and end of STORE. The DSP can read from M2 whenever STORE is absent, by writing the desired channel number S[4:0] to ($A=3$), which selects a specific transceiver to put M2 data on a bus to the Altera chip. Writing the address of the first M2 location to ($A=2$) sets the M2 read pointer.

The DSP can then read a sequence of M2 data words from ($A=0$) or ($A=1$), with no wait states, reading no faster than every third instruction, or once every 100 ns, to allow time for the address to increment, and new data to appear at the DSP.

Setting S7 = 1 in RUN mode disables writing from R1 to M1, allowing a test pattern written into M1 to generate a trigger. In TEST mode, the 10 MHz clock and STORE are disabled and any operation is allowed. The DSP can read or write M1 or M2, with several DSP wait states required for writing.

4.2. Trighost module

The Trighost module is the host for backplane communications with FADC modules, a slave port on the cable bus linking the FADC crate to the outside world, and the trigger processor for the local crate. The module consists of a Motorola DSP56309, four Altera PLDs, and several BTL transceivers (DS3896 and DS3897) for communication over cable and backplane. The DSP has a peripheral interface called the hostport, with 8 data bits and a few control pins, connected to the external cable through trapezoidal BTL transceivers.

Through this cable the MLink module provides hardware reset, initial program load and a variety of communication functions. In addition to DMA block transfers that require little CPU activity from either host or slave DSP, the architecture allows the slave to signal the host through flags, and allows the host to force specified interrupt service. The Trighost DSP is in turn the host of the crate backplane, with the hostports of the 16 FADC module DSPs simply connected though similar transceivers. An Altera EPM7128E PLD, connected to the external memory bus of the Trighost DSP, provides the logic required for the host. With internal DMA controllers, the DSP can simultaneously transfer data on the two busses at their full capacity, with little CPU time.

The Trighost module receives the horizontal and vertical profiles: a total of 32 threshold comparisons, updated every 100 ns. A shower signal appears as light sweeping across the phototube array, appearing in one analog sum as it disappears from a neighboring sum, but moving in either direction with a time scale that varies from shower to shower. A first stage trigger doubles the apparent pulse widths, using 6-bit counters that increment when the signal is above threshold, decrement otherwise and are prevented from overflow and underflow. Requiring that a counter and either of its immediately higher neighbors be simultaneously nonzero provides a loose two-fold coincidence. Repeating the process with another layer of 6-bit counters and coincidence logic provides a loose three-fold space-time coincidence. To reduce the time expansion of coincident pulses, each coincidence stage is gated by the prompt OR of the contributing threshold comparisons.

Trigger processing uses two identically programmed Altera EPF8452A PLDs to carry out the coincidence logic described above, providing two sets of 14-bit coincidence patterns to a third EPF8452A PLD. Each input coincidence bit sets a corresponding flip-flop. The first coincidence starts the trigger and stores its 13-bit time. When the elapsed trigger time reaches 102.4 μs, or a preset interval elapses without subsequent coincidences, a trigger is generated and five numbers are buffered for readout: two 14-bit coincidence patterns, the 13-bit times of the first and last coincidence, and a 13-bit number consisting of 4-bit coincidence counts for each of the 14-bit patterns, and a 5-bit trigger code with separate bits for: at least two 3-fold in at least one view; at least one 3-fold in each view; at least three 3-fold in at least one view; at least two 3-fold in each view; and at least three 3-fold in each view.

If only a single 3-fold coincidence bit is set, no trigger code bits are set, and a trigger is generated

only if it is the first trigger modulo 8, in other words this uninteresting trigger is prescaled by 8. The trigger code least discriminating against noise requires a single 4-fold coincidence.

The Trighost DSP has an 80 MHz clock, unrelated to the 10 MHz measurement clock, but sends two signals to its 16 slaves over the crate backplane that must be switched at predetermined cycles of the 10 MHz clock: the 10 MHz clock itself and the STORE level that controls transfer from first to second memory in the FADC modules. To accomplish this, the DSP simply loads a PLD register with the 13-bit system time for update and the two bits specifying the new values for the signal enables. When the time matches, the update occurs properly synchronized, and the DSP is notified by an interrupt.

4.3. Link modules

Two similar modules provide high-speed communication links between systems in the 22 separate buildings. All link modules have a DSP, bi-directional optical fiber links to two neighboring buildings, and a cable bus, all linked to 256K of 16-bit onboard memory through four independent I/O ports. The optical fibers are organized as two independent site-wide unidirectional serial busses, one in each direction.

An MLink module in the control crate of the FADC rack in each of 21 mirror buildings provides a link between two neighboring buildings and the three modules on its cable bus (two Trighost modules and a Power module). The MLink modules all receive the 10 MHz measurement clock with equal timing throughout the site, over optical fibers from Clock modules in the central facility that also provide characters for control and initial program load. The VLink module in the central host VME crate communicates with the central host computer over the VME backplane, with a DMA master interface that shares an I/O port with the cable bus. The cable bus allows the VLink module to communicate with the two Clock modules that distribute the site-wide measurement clock.

The VLink module has a VME slave port to allow access to a family of registers that control its access to external VME memory: defining access to four separate buffers and providing some additional control and status. The master interface transfers data between the internal memory of the host computer and the onboard memory at 20 MB/s, with individual block transfers initiated by the DSP, but with access permission and region defined by the host. The DSP can initiate DMA transfers on either the VME bus or the cable bus, but not at the same time.

A single Altera PLD serves as a memory controller and interface for four independent memory ports: two serial busses, cable bus and DSP. The serial busses and the DSP can each independently communicate with the memory at 30 MB/s, while the cable bus manages 10 MB/s. Memory access is 60 MHz word rate (120 MB/s), allowing the four channels independent interleaved memory access with no interference. DSP communications with the PLD use only two address bits. Writing to ($A=0$) selects a 4-bit channel number. Channels 0–7 specify the four memory ports and access direction. Higher channels specify timer and external pulse interrupts. Direct read/write access to one of eight separate address counters uses ($A=2$). Writing commands and reading status uses ($A=3$). Data transfers directly to or from the DSP use ($A=1$). Interrupt flags and channel can be read back from ($A=0$).

Serial communications use Cypress HotLink transmitters and receivers, which convert 8-bit CMOS characters to serial ECL and back, using a 30 MHz byte-clock derived from the 60 MHz DSP clock. The ECL serial stream is interfaced to multimode optical fiber for transmission distances up to 100 m. The communication scheme is simple: data packets are preceded by a control character (NULL), followed by a data byte specifying the number of remaining nodes to cross, and bits specifying optional delivery for intermediate nodes. Each receiver is buffered by a FIFO, and all incoming blocks are written to ring buffers in the 256K-word memory. Retransmitted blocks are transmitted as they are received, with a few character delay, after decrementing the node count in the routing header.

To transmit locally originated blocks, the link DSP requests transmission after the block is in memory and the transmitter memory address counter is correctly set, and awaits an interrupt at the end of the transmission. The transmission will not start until the link is idle, but is not interruptible once underway. The maximum packet size is 16-bit header followed by 64 16-bit words. The first "data" word contains a 6-bit count of the number of remaining words. At 30 MB/s, the maximum packet time is under 5 μs, and packets broadcast for trigger communications require less than one μs. Transmission delay is less than 500 ns per node for fiber delay less than 300 ns. For an event with 42 mirrors, each generating a trigger at the same time, all 22 links receive all trigger packets within 50 μs.

DSP access to memory requires writing the DSP port and direction to ($A=0$), writing the first memory address to ($A=2$), and then reading or writing ($A=1$) no faster than once every 67 ns. There are no interrupts or flags associated with DSP access to external memory.

For the cable bus, there are two modes of operation: one with a block transfer to or from memory, with word count in the first word transferred, and an interrupt when the transfer is complete; and a second mode exchanging a single byte. This second mode is used for control and initial program load. When no cable bus communications are underway, the PLD can monitor the cable bus and interrupt the DSP whenever a slave has a transmission request.

The DSP on a link module is thus largely relieved of communications overhead. Transfers to or from the external busses require a few DSP cycles per block. Blocks can be transferred between busses without reading any data into the DSP. The DSP is promptly notified of every block transfer. But DMA transfers can take place at full 30 MB/s on each of the serial busses, 20 MB/s on the VME bus (for the VLink), and 10 MB/s on the cable bus, while the DSP is free to make independent access to the memory or perform computations. Interrupts generated by the completion of a block transfer, errors or the timer are distinguished by reading ($A=0$) to get interrupt status bits.

4.4. Power module

The Power module is in the control crate of each FADC rack and is a slave module on a cable bus hosted by the MLink module. With external AC power available to the rack, both modules are powered. The Power module controls the AC power to the rest of the rack, controls and monitors HV and low voltage power, controls and monitors the door, monitors and influences temperatures. Most of the digital logic is in an Altera 8452 PLD. The DSP communications use only the two lowest-order address bits.

Since some of the elements controlled by the Power module have the ability to damage the detector if improperly operated, we have built in several safeguards. If an open door during daylight permits the sun to be imaged on a cluster, the UV filter and phototubes are promptly destroyed. If HV is present on the cluster at moderately high light levels the tubes age quickly. Even powering electronics during the heat of a summer day can damage equipment.

Control of power has a strict hierarchy: power is controlled by the PLD of the Power module, which is controlled by the Power module DSP, which is controlled by the MLink, which in turn is controlled by optical fiber communications from the central facility. Loss of these communications, perhaps from loss of power in the central facility or damage to an optical fiber, generates a hard reset to the MLink and Power modules, disabling all controllable power. The DSP code in the Power module has a watchdog timer that shuts everything down if no communications are received from the central facility within a 5 min period. The PLD has a watchdog timer that disables power if the DSP fails to access the PLD for a period exceeding 60 ms.

Each building has a light sensor mounted outside next to the rollup door, and a three-position light switch beside the entrance door. Unless the light switch is in its enable position and outside light levels are low, the HV power supplies are disabled and the Power module may not open the door. If the switch is enabled, outside light detected and the door has not engaged its lower

limit switch, the door is automatically closed by PLD logic, regardless of DSP action.

To enable a power function requires a complex series of DSP actions in proper order. If, for example, the HV is momentarily disabled by the enabling light switch or detection of light, the HV may only be restored by a slow complex sequence of setting enables, first for the AC to the supply, then a separate HV enable to the supply, followed by extremely complex sequences required to raise the voltage and current limits from zero. To further guard against accidental action, there are no single code sequences capable of turning on HV from a reset state. Several sequences must be individually requested from the central facility, in proper order.

The central facility has uninterruptible power supply (UPS) protection from AC failure, with almost an hour of battery backup. A separate UPS, with sufficient battery capacity to operate the mirror buildings at full power for several minutes and then safely close all doors, can be remotely monitored and controlled through an optical fiber Ethernet link. Ordinarily, whenever power is present the MLinks and Power modules are operating and monitoring, even if the FADC crates are not powered. At the end of a running period, after verifying that all doors are closed, we can remotely power down the UPS that supplies AC power to all mirror buildings.

Altogether, the Power module monitors 35 analog voltages within the rack, representing power supply voltages or currents and temperatures of crates and supplies. The voltages of the low-voltage supplies are measured at the supply and at the load. All measurements are performed several hundred times per second, allowing detection of transients in the power. Summaries are transmitted to the central facility, usually at 10 s intervals. The Power module also monitors the status of the light sensor, enabling light switch and the limit switches of the rollup door.

The temperature within the rack can be stabilized during running with the aid of a small heat exchanger that can be directly operated by the DSP or through a digitally controlled thermostat. The temperature in the clusters can be stabilized in cold weather by enabling 48VDC to heater strips in the clusters. The Power module monitors voltages, temperatures, and light levels within the cluster and controls a 32-channel test pulser.

4.5. Clock module

The clock module has 12 AMD TAXI transmitters that send a continuous 10 MHz clock to the Link modules. The clock is continuous, maintained by transmitting characters at 10 MB/s, with framing and phase-locked-loops maintained by transmission of NULL characters in the absence of data. The PLD that controls these transmitters has four registers accessible to the DSP:

(1) 12-bit selection pattern;
(2) TAXI data register: 9 bits (high-order 9th bit signals command at LINK) readback is 9-bit character, plus status: d11 means timer set and awaiting match, d12 means data byte awaiting transmission;
(3) 13-bit time, driven by 10 MHz clock;
(4) 13-bit timer, generates interrupt and transmission after time equal.

Writing a 9-bit character to $A=1$ transmits the character over the selected TAXI transmitters, either promptly (within a few 100 ns clock cycles) or at the next timer interrupt, if a timer interrupt is pending. All transmitters continuously transmit NULL characters every clock cycle, except when transmitting data. To transmit data with the timer, load timer ($A=3$) with a safely distant time and then load data ($A=1$). To transmit a timed sequence, with the timer and data set in an interrupt routine, start the sequence by setting the timer to a safe time initially.

There are two interrupts: IRQA when the 13-bit counter wraps, and IRQB when timer and time match for the first time after writing to $A=3$. In use, the 10 MHz input is initially disabled, and the 13-bit counter and the software time counters are initialized. Then the 10 MHz clock is enabled to allow the phase-locked loops of the TAXI transmitters and receivers to achieve lock and the receivers to determine byte boundaries from the NULL transmissions.

4.6. Cluster board

The Cluster board mounts in the top of the back enclosure of the cluster box. DC power from the FADC rack is fused and redistributed. Slow (250 kHz) serial communication with the Power module in the FADC control crate is used to generate test pulses of variable amplitude and width on a selectable subset of 32 coaxial cables connected to the backplane. Each cable provides a test pulse to a set of eight phototubes sharing a signal cable to FADC crate. The temperatures and light levels of four phototubes with modified bases can be read out, along with the temperature and voltage of the Cluster board.

4.7. Modular power supply

We have provided a quiet, low-cost, efficient, compact power supply for the FADC racks. Each unit contains three or four modular DC–DC power supplies manufactured by the Vicor Corporation. The digital electronics in one FADC crate require approximately 50 A of +5 V, which is provided by an 80 A module. The analog signal processing requires a few amperes of +6 V, which is regulated on the FADC board to provide stable +5 V for the FADC and DAC chips. The amplifiers on the FADC board and in the tube bases require approximately 20 A of +5 and −5 V. The CMOS logic on the FADC board provides a very noisy fluctuating load, which is filtered by capacitance on the boards. The power for analog processing uses low dropout regulators on each FADC board, and RC filtering in the tube bases. The Vicor modular power supplies are switching supplies, but use a fairly quiet "zero current switching" of individual 1 μs single cycle sine waves. A full-wave rectifier module supplied by Vicor charges a 600 μF capacitor bank to approximately 300VDC with 208VAC input, using a series resistor to limit initial current before enabling the DC–DC converters.

The supplies are connected to the controlling Power module by a single 26-conductor flat cable. There are three supplies in each rack, labeled A, B, and C. The A and B supplies power the upper and lower FADC crates. The C supply provides a maximum of 10 A of +5 V to the control crate, and a maximum of 200 W of 48VDC to heater strips in the phototube cluster boxes. The control cable provides six separate enables for the analog, digital, and heater power (control power is always enabled). Each unit contains an 8-input ADC (Analog Devices AD7890), which uses serial communication with the host. The serial communications require a single clock and single data line from the Power module, and a serial data line returning from each of the 3 supplies. We cycle though a full set of 8 measurements per module several hundred times per second to monitor fluctuations. We measure the voltage at each supply module, and at the load, using four channels in the C module to measure the +5 and −5 V at the two cluster boxes.

The power supplies are approximately 2 in. thick, 8 in. wide and 14 in. long, and fit between the crates and the side wall of the rack, allowing short power cables to each crate, with Hypertronics quick-disconnect connectors at the crate that are rated for much higher currents and 100K insertion cycles. Heat is removed from the power supply by conduction. The modular supplies are in good thermal contact with an aluminum baseplate, which is bolted through the rack wall to aluminum cooling fins on the outside of the rack. The supplies shut down automatically if their temperatures reach 85°C, but dissipating about 100 W for a 1 kW load, they never reach 75°C on summer nights. We monitor temperatures in the crates and supplies with temperature-to-current transducers (Analog Devices AD592, 1 μA/°K), measuring the current in the Power module.

5. Software architecture

We have 759 DSPs distributed in 22 buildings at a remote site. Within each building, a link module is the top of a tree hierarchy for control and communication. The link modules communicate freely with each other, but the link in the central facility, the VLink module, has supervisory control over the links in the mirror buildings. The six different module types with DSPs have six different programs, but with common features. All are short

assembly language programs, ranging in size from a thousand to a few thousand instructions. All DSPs execute buffered lists of tasks in foreground loops. The tasks are generated primarily in interrupt routines, with stimuli ranging from external pulses to incoming data packets. The task buffers contain pointers to packets that have been received or internally generated. Tasks with different priorities or scheduling constraints form separate lists: generally input and output queues. Interrupts by the DSP internal timer provide a check that tasks are proceeding and help schedule time-critical trigger activity.

Any module in the tree hierarchy can issue a hard reset to modules below. The mirror links are reset by either a reset command on the clock fiber from the central facility to a mirror link, or loss of clock fiber communications, perhaps a result of power loss in the central VME crate or a rodent gnawing through a clock fiber. Resetting a mirror link also resets the power module and turns off power to the two FADC crates in the rack. After reset, a powered module may be booted up with an initial program load from its master, followed by additional configuration information.

The VME PC is the immediate master of the VLink. When communications with the VLink are established, the VLink boots and configures the clock modules, which in turn boot up the link modules in the mirror buildings. The mirror links are configured by the VLink over the serial bus and then they in turn boot and configure the power modules. All commands, program code and configuration data originate on the VME PC.

Communications are in formatted packets of 16-bit numbers. The first word is an identifier containing a 6-bit count of following words, including the first word repeated at the end of the packet. For packets headed down the tree, the packet contains routing information. The destination of packets headed up the tree is implicit in the packet type. When transmitted over a serial bus, the packet is preceded by an additional word specifying the number of nodes to cross, and whether intermediate nodes are to receive the packet. The two serial busses are treated differently: one is reserved for data communications between the VLink and individually requested mirror links. The other is for short trigger packets and messages spontaneously generated within mirror buildings or the central facility. Each link has separate input and output queues for each serial direction.

6. Conclusion

Stereo observations of cosmic ray showers, using telescopes at two sites at Dugway Utah, have been underway since construction of the High Resolution Fly's Eye was completed in the fall of 1999. The data acquisition system installed at the newest site is based on FADC electronics designed at Nevis Laboratories, and performs as expected, with appropriate reliability, sensitivity and measurement detail.

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References

[1] R.M. Baltrusaitis, et al., Nucl Instr. and Meth. A 240 (1985) 410.
[2] J.H.V. Girard, et al., Nucl. Instr. and Meth. A 460 (2001) 278.
[3] L.R. Wiencke, et al., Nucl. Instr. and Meth. A 428 (1999) 593.
[4] B.F. Jones, et al., Proceedings of the 26th ICRC, Vol. 5, 1999, p. 429.
[5] T. Abu-Zayad, et al., Proceedings of the 25th ICRC, Vol. 7, 1997, p. 213.